THIN FILM TRANSISTOR ARRAY SUBSTRATE FOR A LIQUID CRYSTAL DISPLAY AND METHOD FOR FABRICATING THE SAME

BACKGROUND OF THE INVENTION

(a) Field of the Invention

The present invention relates to a thin film transistor array substrate for a liquid crystal display and, more particularly, to a thin film transistor array substrate for in-plane switching type liquid crystal displays.

(b) Description of the Related Art

Recently, a twisted nematic (TN) mode has been applied to liquid crystal displays in a most extensive manner. In the TN mode, electrodes are provided at the two substrates while interposing the liquid crystal, and the longitudinal molecular axes (the so-called directors) of the liquid crystal are twisted by 90 ° with respect to the substrates. When voltages are applied to the electrodes, the directors of the liquid crystal are driven. Such a TN mode bears a narrow viewing angle, however. In this connection, in-plane switching (IPS) typed liquid crystal displays have been developed to replace for the TN mode liquid crystal displays. U.S. Patent No. 5,598,285 discloses such an in-plane switching typed liquid crystal display.

However, in such an in-plane switching typed liquid crystal display, potential difference is made between the data line and the neighboring pixel or common electrodes so that light leaks at the periphery of the data line. The light leakage is directly seen from the lateral side, causing a lateral cross talk.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide an in-plane switching type liquid crystal display with minimum leakage of light.

These and other objects may be achieved with the following structure. In a thin film transistor array substrate for the in-plane switching type liquid crystal display, light interception patterns are formed at the same plane as the semiconductor patterns such that they are overlapped with data lines as well as pixel or common electrodes positioned close to the data lines.

According to one aspect of the present invention, the thin film transistor array substrate includes a plurality of gate lines formed at a transparent insulating substrate, and a plurality of data lines crossing over the gate lines in a matrix form to define pixel regions while being insulated from the gate lines. Common electrodes and pixel electrodes are placed at the pixel regions while being spaced apart from each other with a predetermined distance. Thin film transistors are electrically connected to the gate and the data lines. Each thin film transistor has a silicon-based semiconductor pattern. A light interception pattern is formed at the same plane as the semiconductor pattern with the same material.

The light interception pattern overlaps with the corresponding data line, and the common or the pixel electrodes positioned close to the data line. It is preferable that the light interception pattern is overlaps with the common or the pixel electrodes placed at the neighboring pixel regions.

The semiconductor pattern is connected to the corresponding light interception pattern, and extended to the bottom of the corresponding data line. The light

interception pattern may be extended external to the periphery of the corresponding data line.

The pixel or common electrodes are formed at the same plane as the gate or data lines, or at the plane different from the gate or data lines.

According to another aspect of the present invention, the thin film transistor array substrate includes an insulating substrate, and a gate line assembly formed on the substrate. The gate line assembly has gate lines, and gate electrodes connected to the gate lines. Linear common electrodes are formed on the substrate while being separated from the gate line assembly. A gate insulating layer covers the gate line assembly and the common electrodes. Semiconductor patterns are formed on the gate insulating layer over the gate electrodes. Light interception patterns are formed on the gate insulating layer. The light interception pattern is formed with the same material as the semiconductor pattern. A data line assembly is formed on the substrate. The data line assembly has source and drain electrodes formed on the semiconductor patterns, and data lines connected to the source electrodes. The data lines crosses over the gate lines in a matrix form to define pixel regions. Linear pixel electrodes are formed at the pixel regions such that they are alternated with the common electrodes. The pixel electrodes are electrically connected to the drain electrodes.

A protective layer may cover the data line assembly while bearing contact holes. The pixel electrodes are formed on the protective layer such that they are connected to the drain electrodes through the contact holes.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete appreciation of the invention, and many of the attendant

advantages thereof, will be readily apparent as the same becomes better understood by reference to the following detailed description when considered in conjunction with the accompanying drawings in which like reference symbols indicate the same or the similar components, wherein:

Fig. 1 is a plan view of a thin film transistor array substrate for an in-plane switching type liquid crystal display according to a first preferred embodiment of the present invention;

Fig. 2 is a cross sectional view of the thin film transistor array substrate taken along the II-II' line of Fig. 1;

Figs. 3A, 4A and 5A are plan views illustrating the steps of fabricating the thin film transistor array substrate shown in Fig. 1 in a sequential manner;

Figs. 3B, 4B and 5B are cross sectional views of the thin film transistor array substrate taken along the IIIb-IIIb' line of Fig. 3A, the IVb-IVb' line of Fig. 4A, and the Vb-Vb' line of Fig. 5A, respectively;

Fig. 6 is a plan view of a thin film transistor array substrate for an in-plane switching type liquid crystal display according to a second preferred embodiment of the present invention;

Fig. 7 is a cross sectional view of the thin film transistor array substrate taken along the VII-VII' line of Fig. 6;

Figs. 8 to 12 sequentially illustrate the steps of fabricating the thin film transistor array substrate shown in Fig. 6 after the processing step illustrated in Figs. 3A and 3B;

Fig. 13 is a plan view of a thin film transistor array substrate for an in-plane switching type liquid crystal display according to a third preferred embodiment of the

present invention;

Fig. 14 is a cross sectional view of the thin film transistor array substrate taken along the XIV-XIV' line of Fig. 13;

Figs. 15 to 17 sequentially illustrate the steps of fabricating the thin film transistor array substrate shown in Fig. 13 after the processing step illustrated in Figs. 3A and 3B;

Figs. 18A and 19A are plan views sequentially illustrating the steps of fabricating the thin film transistor array substrate shown in Fig. 13 after the processing steps illustrated in Fig. 17; and

Figs. 18B and 19B are cross sectional views of the thin film transistor array substrate taken along the XVIIIb-XVIIIb' line of Fig. 18A, and the XIXb-XIXb' line of Fig. 19A, respectively.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of this invention will be explained with reference to the accompanying drawings.

Fig. 1 is a plan view of a thin film transistor array substrate for an in-plane switching type liquid crystal display according to a first preferred embodiment of the present invention, and Fig. 2 is a cross sectional view of the liquid crystal display taken along the II-II' line of Fig. 1.

As shown in the drawings, a gate line assembly and a common line assembly are formed on an insulating substrate 10. The gate line assembly and the common line assembly are single or multiple-layered with a metallic or conductive material such as Al or Al alloy, Mo or MoW alloy, Cr, and Ta. The gate line assembly includes gate lines 22

proceeding in the horizontal direction, and gate electrodes 26 connected to the gate lines 22 to form thin film transistors (TFTs). The gate line assembly may further include gate pads (not shown) for receiving scanning signals from the outside and transmitting the signals to the gate lines 22. The common line assembly includes common signal lines 28 proceeding parallel to the gate lines 22, and common electrodes 27 and 271 connected to the common signal lines 28 to receive common signals via the common signal lines 28. The common line assembly 27 and 28 may be overlapped with a pixel line assembly 67 and 68 to be described later to function as an electrode for a storage capacitor.

A gate insulating layer 30 is formed on the entire surface of the substrate 10 with silicon nitride while covering the gate line assembly 22 and 26, and the common line assembly 27 and 28.

Island-like semiconductor patterns 40 are formed on the gate insulating layer 30 over the gate electrodes 26 with amorphous silicon. Light interception patterns 44 are formed on the gate insulating layer 30 with the same material as the semiconductor patterns 40 such that the edge portions thereof are overlapped with the two neighboring common electrodes 271 and the two neighboring common signal lines 28 placed at the peripheral portions of the pixels. In this case, as the common electrodes 271 are positioned close to data lines 62 to be described later, the light interception patterns 44 are overlapped with the common electrodes 271. In contrast, when pixel electrodes 67 are positioned close to the data lines 62, the light interception patterns 44 may be overlapped with the pixel electrodes 67.

First and second ohmic contact patterns 55 and 56 are formed on the

semiconductor patterns 40 with n+ hydrogenated amorphous silicon doped with n-type impurities at high concentration such that they are separated centering around the gate electrodes 26. Third ohmic contact patterns 52 are formed on the light interception patterns 44 such that they are connected to the first ohmic contact patterns 55.

A data line assembly and a pixel line assembly are formed on the ohmic contact patterns 52, 55 and 56, and the gate insulating layer 30. The data line assembly and the pixel line assembly are single or multiple-layered with a metallic material such as Cr, Mo-W alloy, Al and Al alloy, or indium tin oxide (ITO). The data line assembly includes data lines 62 crossing over the gate lines 22 in a matrix form while overlapping the light interception patterns 44, source electrodes 65 connected to the data lines 62 while extending toward the gate electrodes 24, and drain electrodes 66 separated from the data lines 62 while facing the source electrodes 65 centering around the gate electrodes 26. The data line assembly may further include data pads (not shown) connected to one end of the data lines 62 to receive picture signals from the outside. The pixel line assembly includes pixel signal lines 68 proceeding in the horizontal direction while being connected to the drain electrodes 66, and pixel electrodes 67 proceeding parallel to the common electrodes 27 and 271 while being connected to the pixel signal lines 68. The pixel signal lines 68 are overlapped with the common signal lines 28 to form storage capacitors.

A protective layer 70 is formed on the substrate 10. The protective layer 70 may have contact holes exposing the gate and data pads. A subsidiary data line assembly may be formed on the protective layer 70 such that it is connected to the data line assembly, and subsidiary pads may be also formed on the protective layer 70 such

that they are electrically connected to the pads.

In this structure, the light interception patterns 44 may prevent light leakage between the data line 62 and the common electrodes 271 close thereto, thereby preventing a lateral cross talk. Particularly, it is important that the light interception patterns 44 are formed with the same material as the semiconductor patterns 40. If the light interception patterns 44 are formed with a metallic material bearing higher reflexibility, light is repeatedly reflected in-between the metallic light interception pattern and the data line 62 or the common electrodes 271. The resulting light leakage induces lateral cross talk.

The way of forming the light interception patterns 44 and the semiconductor patterns 40 at the same plane may be also applied to twisted nematic liquid crystal displays.

A method for fabricating the thin film transistor array substrate shown in Fig. 1 will be now described in detail.

Figs. 3A to 5B illustrate the steps of fabricating the thin film transistor array substrate in a sequential manner.

As shown in Figs. 3A and 3B, a metallic layer having a thickness of about 3000 Å is deposited onto a transparent insulating substrate 10, and patterned through photolithography using one mask to thereby form a gate line assembly and a common line assembly. The gate line assembly includes gate lines 22 and gate electrodes 26, and the common line assembly includes common signal lines 28 and common electrodes 27 and 271.

Thereafter, as shown in Figs. 4A and 4B, a gate insulating layer 30 is deposited

onto the substrate 10 with silicon nitride or organic insulating material to a thickness of 3000-5000 Å. An amorphous silicon layer 40 with a thickness of about 500-2000 Å, and a doped amorphous silicon layer 50 containing impurities such as phosphorous with a thickness of about 500 Å are deposited onto the gate insulating layer 30 in a sequential manner. The doped amorphous silicon layer 50 and the underlying amorphous silicon layer 40 are patterned together through photolithography using one mask to thereby form island-shaped semiconductor patterns 40 and light interception patterns 44, and ohmic contact patterns 50 and 52 thereon. The semiconductor patterns 40 are placed over the gate electrodes 26, and the light interception patterns 44 are respectively placed between the two neighboring common electrodes 271 centering around a data line 62 that will be formed later. At this time, the amorphous silicon layer 40 may be additionally left on the gate insulating layer 30 where the data lines 62 cross over the common electrode lines 28, and the gate lines 22.

As shown in Figs. 5A and 5B, a metallic layer with a thickness of 2000-5000 Å is deposited onto the substrate 10 with Cr, Al alloy, Mo, or Mo alloy, and patterned through photolithography using one mask to thereby form a data line assembly and a pixel line assembly. The data line assembly includes data lines 62 crossing over the gate lines 22, and source and drain electrodes 65 and 66. The pixel line assembly includes pixel signal lines 68, and pixel electrodes 67. Then, the ohmic contact patterns 50 exposed through the data line assembly are etched such that they are separated centering around the gate electrodes 26. In this way, the ohmic contact patterns 55 and 56 are completed. At this time, the portions of the ohmic contact patterns 52 on the light interception patterns 44 that are not covered by the data lines

62 are also etched.

Thereafter, as shown in Figs. 1 and 2, a protective layer 70 is formed on the entire surface of the substrate 10 by depositing silicon nitride or organic insulating material thereon.

Thereafter, the steps of forming contact holes exposing the gate line assembly or the data line assembly through patterning the protective layer 70, and forming a subsidiary data line assembly and subsidiary pads through depositing a conductive layer onto the protective layer 70 and patterning it may be additionally performed.

Meanwhile, even if the semiconductor patterns and the data line assembly are formed through photolithography using one mask to simplify the overall processing steps, the light interception patterns may be formed at the same plane as the semiconductor patterns.

Fig. 6 is a plan view of a thin film transistor array substrate for an in-plane switching type liquid crystal display according to a second preferred embodiment of the present invention, and Fig. 7 is a cross sectional view of the thin film transistor array substrate taken along the VII-VII' line of Fig. 6.

As shown in the drawings, a gate line assembly 22 and 26, a common line assembly 27, 271 and 28, a data line assembly 62, 65 and 66, and a pixel line assembly 67 and 68 have the same structure as those related to the first preferred embodiment.

The difference is made in that semiconductor patterns 42 have the same shape as the data line assembly 62, 65 and 66 except channel portions for TFTs. Furthermore, light interception patterns 44 are connected to the semiconductor patterns

42 below the data lines 62, and ohmic contact patterns 55 and 56 are formed with the same shape as the data line assembly 62, 65 and 66.

A method for fabricating the thin film transistor array substrate shown in Fig. 6 will now be described with reference to Figs. 8 to 12.

First, as shown in Figs. 3A and 3B, a gate line assembly 22 and 26, and a common line assembly 27, 271 and 28 are formed in the same way as in the first preferred embodiment.

Then, as shown in Fig. 8, a gate insulating layer 30 with a thickness of 1500-5000 Å, a semiconductor layer 40 with a thickness of 500-2000 Å, and an ohmic contact layer 50 with a thickness of 300-600 Å are sequentially deposited onto the substrate 10 through chemical vapor deposition. Thereafter, a conductive layer 60 with a thickness of 1500-3000 Å is deposited onto the ohmic contact layer 50 through sputtering. And a photoresist film 110 is coated onto the conductive layer 60 to a thickness of 1-2.

Thereafter, as shown in Fig. 9, the photoresist film 110 is exposed to light through a second mask, and developed to thereby form first and second photoresist patterns 112 and 114. At this time, the first photoresist pattern 114 placed at the channel portion C between source and drain electrodes 65 and 66 as well as the portion C where light interception patterns 44 are formed has a thickness smaller than that of the second photoresist pattern 112 placed at the portion A where the data line assembly 62, 65 and 66 and the pixel line assembly 67 and 68 are formed. The thickness ratio between the first photoresist pattern 114 at the C portion and the second photoresist pattern 112 at the A portion varies depending upon subsequent processing

conditions. It is preferable that the thickness of the first photoresist pattern 114 is a half or less the thickness of the second photoresist pattern 112. Furthermore, it is preferable that the second photoresist pattern 112 has a thickness of 1.6-1.9, and the first photoresist pattern 114 has a thickness of 2000-5000 Å, or more preferably of 3000-4000 Å. In case a positive photoresist film is used to form such photoresist patterns 112 and 114, it is preferable that the mask for photolithography has a light transmission of 3% at portion A, a light transmission of 20-60%, or more preferably of 30-40% at portion C, and a light transmission of 90% or more at the remaining portion B.

Although various techniques may be applied in positionally differentiating the thickness of the photoresist film, two techniques will be introduced here when a positive photoresist film is used. For the processing convenience, the thickness of the photoresist film is preferably set to be in the range of 1.6-2, which is thicker than usual.

In the first technique, slit or lattice patterns, or semi-transparent films are provided at the mask to control the degree of light exposure. The patterning width or pitch is set to be smaller than the decomposition capacity of the light exposing device. Meanwhile, when a semi-transparent film is used in the mask, the film thickness may be varied to control the light transmission. Alternatively, a plurality of films of different thickness may be used to control the light transmission. Cr, MgO, MoSi, a-Si, etc. may be used to control the degree of light exposure.

When the photoresist film is exposed to light through the mask with slit patterns or a semi-transparent film, the degrees of molecular decomposition in the photoresist film became different between the patterned portion and the non-patterned portion.

However, it should be noted that too long exposure may completely remove the photoresist film. When the photoresist film exposed to light is developed, the non-exposed portion almost keeps the initial thickness. The portion slightly exposed to light through the slit pattern or the semi-transparent film bears a middle thickness. And the portion completely exposed to light has nearly no thickness. In this way, the photoresist patterns 112 and 114 of partially different thickness may be made.

The second technique is based on reflow of the photoresist film. In this technique, a usual mask with a transparent portion and an opaque portion is used to form a usual photoresist pattern. In the photoresist pattern, the film portion is partially flown into the non-film portion while forming a second film portion with a middle thickness.

In these ways, the photoresist patterns 112 and 114 of positionally different thickness are made.

Then, the photoresist patterns 112 and 114, and the underlying conductive layer 60, ohmic contact layer 50, and semiconductor layer 40 are sequentially etched. At this time, the data line assembly and the underlying layers are left at the A portion, only the semiconductor layer is left at the C portion, and the gate insulating layer 30 is exposed to the outside at the remaining B portion.

Specifically, as shown in Fig. 10, the conductive layer 60 at the B portion is removed while exposing the underlying ohmic contact layer 50 at this process, dry etching or wet etching is used in such a condition that the conductive layer 60 is etched, and the photoresist patterns 112 and 114 are not nearly etched. However, as the dry etching, is difficult to find such a selective etching condition, the photoresist patterns

112 and 114 may be etched together, provided that the thickness of the first photoresist pattern 114 is so large that the underlying conductive layer 60 is not exposed through the dry etching.

When the conductive layer 60 is formed with Mo or MoW alloy, Al or Al alloy, or Ta, either the dry etching or the wet etching may be applied. However, since Cr is not well removed through the dry etching, the wet etching is preferably applied to the Cr-based conductive layer 60. In the wet etching, $CeNHO_3$ may be used as the etching solution. In the dry etching, a mixture of CF_4 and HCl or CF_4 and O_2 may be used as the etching gas.

Consequently, as shown in Fig. 10, only the conductive pattern 69 at the portion A and the portion C is left, and the conductive layer 60 at the remaining portion B is all removed while exposing the underlying ohmic contact layer 50. The conductive pattern 69 has the same shape as the data line assembly 62, 65 and 66 except that the source and drain electrodes 65 and 66 are not separated from each other. Furthermore, in the case of dry etching, the photoresist patterns 112 and 114 are partially etched at some degree.

Thereafter, the exposed ohmic contact layer 50 at the B portion and the underlying semiconductor layer 40 are removed through dry etching together with the first photoresist pattern 114. The etching condition is that the photoresist patterns 112 and 114, the ohmic contact layer 50 and the semiconductor layer 40 are etched together (the semiconductor layer and the ohmic contact layer has almost the same etching selection property) while the gate insulating layer 30 being not etched. Particularly, it is preferable that the etching degrees with respect to the photoresist

patterns 112 and 114 and the semiconductor layer 40 are nearly the same. For example, with the use of a mixture of SF_6 and HCL or a mixture of SF_6 and O_2, the two layers can be etched by nearly the same thickness. In case the etching degrees with respect to the photoresist patterns 112 and 114 and the semiconductor layer 40 are identical with each other, the thickness of the first photoresist pattern 114 is the same as or less than the sum in thickness of the semiconductor layer 40 and the ohmic contact layer 50.

As shown in Fig. 11, the first photoresist pattern 114 at the C portion is removed while exposing the conductive pattern 69. And the ohmic contact layer 50 and the semiconductor layer 40 at the B portion are removed while exposing the gate insulating layer 30. Meanwhile, the second photoresist pattern 112 at the A portion is also etched and partially reduced in thickness. Furthermore, in this step, the semiconductor patterns 42 and the light interception patterns 44 are completed.

The photoresist residue at the C portion is removed through ashing. Plasma gas or microwave may be used for the ashing, and oxygen is the main content of the ashing composition.

As shown in Fig. 12, the conductive pattern 69 at the C portion and the underlying ohmic contact pattern 50 are removed through etching. Dry etching may be applied to all of the conductive pattern 69 and the ohmic contact pattern 50. Alternatively, wet etching may be applied to the conductive pattern 69 while dry etching being applied to the ohmic contact pattern 50. In the former case, the etching is preferably performed under the condition that the etching selection ratios of the conductive pattern 69 and the ohmic contact pattern 50 are large. In case the etching

selection ratios are not large, it is difficult to find the final point of etching and control the thickness of the semiconductor pattern 42 and the light interception pattern 44 to be left at the C portion. For instance, the conductive pattern 69 may be etched using the mixture of SF_6 and O_2. In the latter case where the wet etching and the dry etching are alternatively used, the lateral side of the conductive pattern 69 suffering the wet etching is etched, but that of the ohmic contact pattern 50 suffering the dry etching is not nearly etched so that stepped portions are made. A mixture of CF_4 and HCL or a mixture of CF_4 and O_2 may be used for the ohmic contact pattern 50, the semiconductor pattern 42, and the light interception pattern 44 as the etching gas. With the use of the mixture of CF_4 and O_2, the semiconductor pattern 42 and the light interception pattern 44 may be uniformly made. At this time, as shown in Fig. 7, the semiconductor pattern 42 and the light interception pattern 44 as well as the second photoresist pattern 112 may be reduced in thickness. The etching condition is that the gate insulating layer 30 is not etched. The thickness of the second photoresist pattern 112should be large enough not to expose the underlying data line assembly 62, 65 and 66 through the etching.

Consequently, the source and drain electrodes 65 and 66 are separated from each other while completing the data line assembly 62, 65 and 66 and the underlying ohmic contact patterns 55 and 56.

Finally, the second photoresist pattern 112 at the A portion is removed. However, the second photoresist pattern 112 may be removed before removing the ohmic contact pattern 50 after the conductive pattern 69 at the C portion is removed.

Furthermore, when the data line assembly is formed with a material well adapted to the dry etching, the ohmic contact patterns, the semiconductor patterns and

the data line assembly may be completed through performing only one etching process without establishing several intermediate processing steps. That is, in the etching process, when the metallic layer 60, the ohmic contact layer 50 and the semiconductor layer 40 at the B portion are etched, the first photoresist pattern 114 and the underlying ohmic contact layer 50 at the C portion are etched, and the second photoresist pattern 112 at the A portion is partially etched.

As described above, the wet etching and the dry etching may be alternatively used, or only the dry etching may be used. In the latter case, since only one kind of etching is used, the processing is relatively simple, but it is difficult to find proper etching conditions. By contrast, in the former case, it is relatively easy to find the proper etching conditions, but the processing steps are complicated compared to the latter case.

After the formation of the data line assembly 62, 65 and 66, as shown in Fig. 7, silicon nitride is deposited onto the substrate 10 through chemical vapor deposition, or organic insulating material is spin-coated onto the substrate 10 to thereby form a protective layer 70 with a thickness of 2000 Å or more.

In short, the semiconductor patterns 42 and the data line assembly 62, 65 and 66 may be formed through photolithography using on one mask, thereby simplifying the processing steps. At this time, the semiconductor patterns 42 and the light interception patterns 44 may be formed using the first photoresist pattern 114 with a relatively thin thickness.

Furthermore, the photoresist pattern with a relatively thin thickness is formed only at the channel portion for the TFT, and the light interception pattern connected to

the semiconductor pattern is formed such that it is extended outward of the data line, thereby preventing light leakage at the periphery of the data line.

Fig. 13 is a plan view of a thin film transistor array substrate for an in-plane switching type liquid crystal display according to a third preferred embodiment of the present invention, and Fig. 14 is a cross sectional view of the thin film transistor array substrate taken along the XIV-XIV' line of Fig. 13.

As shown in the drawings, the overall structure of the thin film transistor array substrate is quite similar to the second preferred embodiment.

The difference is that light interception patterns 44 are connected to the semiconductor patterns 42, and extended external to the data line assembly 62, 65 and 66 by the width of a. Furthermore, a pixel line assembly 88 and 87 is formed on a protective layer 70 with contact holes 76, and connected to the drain electrodes 66 through the contact holes 76 of the protective layer 70.

The method of fabricating the thin film transistor array substrate shown in Fig. 13 will be now described with reference to Figs. 15 to 19B.

First, as shown in Fig. 15, first and second photoresist patterns 114 and 112 are made in the same way as in the second preferred embodiment, and the conductive layer 60 is etched using the first and second photoresist patterns 114 and 112 as the etching mask to thereby form a conductive pattern 69.

Thereafter, as shown in Fig. 16, the exposed ohmic contact layer 50 and the underlying semiconductor layer 40 are removed through dry etching while exposing the gate insulating layer 30 and the conductive pattern 69 at the channel portion. At this time, the light interception patterns 44 and the semiconductor patterns 42 are

completed.

As shown in Fig. 17, the first photoresist pattern 114 at the channel portion is entirely removed through etch back to expose the conductive pattern 69. At this time, the second photoresist pattern 112 is partially removed while being reduced in width and thickness and exposing the periphery of the conductive pattern 69.

Thereafter, as shown in Figs. 18A and 18B, the exposed conductive pattern 69 and the underlying ohmic contact layer 50 are etched using the second photoresist pattern 112 as the etching mask. Consequently, the source and drain electrodes 65 and 66 are separated from each other, thereby completing the data line assembly 62, 65 and 66 and the underlying ohmic contact patterns 55 and 56. The width of the light interception pattern 44 extended external to the data line assembly is preferably in the range of 1-3.

After the data line assembly 62, 65 and 66 is completed and the second photoresist pattern 112 is removed, as shown in Figs. 19A and 19B, silicon nitride is deposited onto the substrate 10 through chemical vapor deposition, or organic insulating material is spin-coated onto the substrate 10 to thereby form a protective layer 70 with a thickness of 2000Å or more. The protective layer 70 is patterned through photolithography to thereby form contact holes 76 exposing the drain electrodes 66.

Finally, a conductive layer is deposited onto the protective layer 70, and patterned to thereby form a pixel line assembly 88 and 87 connected to the drain electrodes 66 through the contact holes 76.

A subsidiary data line assembly and subsidiary pads may be additionally

formed at the same plane as the pixel line assembly 88 and 87 such that they are electrically connected to the data lines 62 through the contact holes 76 of the protective layer 70.

As described above, the light interception patterns are formed at the same plane as the semiconductor patterns so that possible leakage of light at the periphery of the data lines is prevented while blocking occurrence of lateral cross talk.

While the present invention has been described in detail with reference to the preferred embodiments, those skilled in the art will appreciate that various modifications and substitutions can be made thereto without departing from the spirit and scope of the present invention as set forth in the appended claims.